Remarks

Applicant appreciates the Examiner's time in discussing the apparent confusion in regard to the § 112(2) rejections and the related lack of correspondence, via telephone with Applicant's undersigned representative, on June 27, 2011. In the following, Applicant has addressed these and other issues, in view of which all rejections are believed improper. Applicant further invites the Examiner to telephone Applicant's undersigned representative, to discuss these matters in advance of any Advisory Action/Appeal.

The Final Office Action dated April 28, 2011, presents the following claim rejections: claim 1 stands rejected under 35 U.S.C. § 112(2); claims 1, 5, 7 and 13 stand rejected under 35 U.S.C. § 103(a) over Thüringer *et al.* (U.S. Patent No. 6,498,404); claims 2-4 stand rejected under 35 U.S.C. § 103(a) over the '404 reference in view of Patterson *et al.*("Computer Architecture: A Quantitative Approach") pp. 134-135, 1995; and claims 6, 8 and 14 stand rejected under 35 U.S.C. § 103(a) over the '404 reference in view of Kitamura *et al.* (U.S. Patent No. 4,212,056). In the following discussion, Applicant does not acquiesce in any regard to averments in the Advisory Action or the Office Actions of record (unless Applicant expressly indicates otherwise).

Applicant believes that the § 112(2) rejection is based upon a misreading of the claims, and is thus inapplicable as asserted. Further, Applicant believes that this misunderstanding is carried through to all § 103(a) rejections, in view of which the rejections are improper as well.

Beginning with the § 112(2) rejection, with respect to the limitations directed to receiving "pairs of processing signals" and the later-recited "pair of processing signals for each of the processing circuits," Applicant finds no clarity issue as asserted, and believes that the Examiner may have overlooked the claims as a whole. In particular, the rejection cites to claim terms reciting a "pair of processing signals," but does so independently from the immediately following terms "for each of the processing circuits." Considering that the claim is directed to a plurality of such processing circuits and a "pair of processing signals" from each circuit, the respective pairs of signals from each circuit may correspond to the "pairs of processing signals" as previously referenced. Applicant thus believes that the claim is clear.

With respect to the Office Action's questions as to whether the recitation of "a combined activity signal" and "a sum of power supply currents" can be the same as or different from previously-discussed signals, Applicant believes that such questions of claim breadth are an improper basis for rejections under § 112(2). As consistent with M.P.E.P. § 2173.04 the "(b)readth of a claim is not to be equated with indefiniteness." *See In re Miller*, 441 F.2d 689 (CCPA 1971). Notwithstanding this, Applicant has amended the claims to replace "a" with "the," in view of which the rejections are believed to be inapplicable.

Applicant respectfully traverses all of the § 103(a) rejections, each of which relies upon the '404 reference, as the '404 reference (alone or as combined) fails to correspond as asserted to the claimed invention "as a whole" (§ 103(a)) including, for example, aspects directed to an activity monitor circuit that receives pairs of processing signals, including a pair of processing signals for each of a plurality of processing circuits within a processing unit. As another example, the Office Action has failed to establish correspondence to aspects directed to deriving a combined activity signal from each of the aforesaid pairs of signals, including a pair for each of the plurality of processing circuits. As such, the rejections fail.

More specifically, the Office Action appears to have confused the cited '404 reference's monitoring of signals for a data processing device, with aspects of Applicant's claimed invention as directed to receiving a pair of signals for each of a plurality of processing circuits, and further combining such received signals to derive a combined activity signal. Referring to page 6 of the Office Action, the Examiner asserts that the cited "data processing device" in the '404 reference corresponds to aspects of the claimed invention directed to a processing unit. Page 7 of the Office Action then goes on to assert that monitoring of the data processing device (as an output signal), together with receiving a power connection as an input signal, corresponds to aspects directed to monitoring pairs of signals from a plurality of processing circuits therein. This assertion is erroneous. First, Applicant fails to understand how the "power connection" and the "power consumption of data processing device" would correspond to aspects of the claimed invention directed to an input and output signal of one of a plurality of processing circuits. Second, the Office Action's assertions stop short of establishing

correspondence, as the cited monitoring of a data processing device fails to correspond to receiving pairs of signals from different processing circuits within such a device. Further, referring to page 9 of the Office Action, the Examiner's assertion that the cited "data processing device, which is a circuit arrangement i.e., has multiple circuits" fails to establish any correspondence to the aforesaid aspects as directed to receiving pairs of signals from a plurality of processing circuits. While the data processing device may have "multiple circuits," the Office Action has not established (or even attempted to assert) that processing signals are received from each of the "multiple circuits" or would be combined.

In view of the above, the Office Action has failed to establish correspondence to various aspects of Applicant's claimed invention, including those directed to an activity monitor circuit coupled to receive a pair of processing signals for each of a plurality of processing circuits, and to combining such signals in providing an indication of power supply that will be consumed by all of the processing circuits in combination. As the Office Action has misapplied the '404 reference in this context, in regard to the rejections of independent claims 1 and 7, all of the rejections are improper and should be removed.

In addition to the above, Applicant submits that the respective 103(a) rejections relying upon the secondary Patterson and '056 references are also improper for lack of correspondence in consideration of the above misinterpretations, as further extending to the proposed combinations (*e.g.*, the alleged motivation is inapplicable as the resulting embodiment does not operate as asserted).

Applicant further traverses the § 103(a) rejections over the '404 reference because the reference itself teaches away from the Office Action's proposed combination. Consistent with the recent *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Applicant maintains that the combination teaches away because the '404 reference integrates its load circuit and data processing device for

security reasons (*see, e.g.*, columns 1:66-67 and 2:1-4), yet the proposed modification would undermine this purpose and render the resulting embodiment vulnerable to attacks as discussed in the '404 reference as those to be avoided. As such, the rejections cannot be maintained.

While the Examiner's response to arguments attempts to rebut this teaching away, it does so in reliance upon an opinion regarding supposed benefits of interchangeability, yet fails to address the teachings in the '404 reference as noted by the Applicant as teaching away, both above and in the (now uncontested) record. In particular, the Examiner's reliance upon M.P.E.P. § 2144.04 in asserting that "making integral things separable is 'merely a matter of obvious engineering choice'" is applied blindly. Such an "engineering choice" cannot stand in contrast to teaching away in the reference itself, consistent with M.P.E.P. § 2143.01 and the above-cited KSR decision. Applicant therefore submits that the proposed combination of references thus lacks motivation, and cannot stand.

Applicant notes that claim 7 has been amended to correct an informality. Specifically, claim 7 has been amended to change a comma to a semicolon, for consistency.

Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the attorney overseeing the application file, Juergen Krause-Polstorff, of NXP Corporation at (408) 474-9062.

Please direct all correspondence to:

Intellectual Property and Licensing
NXP Semiconductors
1109 McKay Drive MS41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____

Robert J. Crawford
Reg. No.: 32,122
Eric J. Curtin
Reg. No. 47,500
651-686-6633
(NXPS.589PA)